

Hewlett Packard Enterprise

THE BRAVE NEW WORLD OF EXASCALE COMPUTING: COMPUTATION IS FREE, DATA MOVEMENT IS NOT

Utz-Uwe Haus, Head of HPE HPC/AI EMEA Research Lab 2021-03-03

TRR154/MINOA conference "Trends in Modelling, Simulation and Optimisation: Theory and Applications"



Supported by the European Union's Horizon 2020 research and innovation program through grant agreement 801101.



HPE HPC/AI EMEA RESEARCH LAB

Deep Technical Collaboration

- HPE & Customers work together
- Focus on new technologies
- Drive future HPE products
- Long term technical relationship



Research Interests

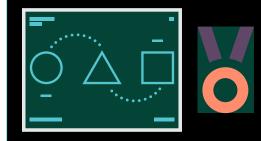
- Memory hierarchy
- Data Movement and Workflows
- Novel accelerators, highly heterogenous systems
- Compilers and mathematical optimisation
- HPC in Cloud, AI and Big Data
- System and site monitoring and data analysis

Engagement

Models

- Advanced Collaboration Centers in Centers of Excellence
- Value Add projects
- EU H2020 research projects





ADVANCED COLLABORATION CENTERS IN EMEA



ARCHER/ARCHER2, UK

- LASSi IO Monitoring and Analytics
- Application tuning (XC30/EX)
- IO Performance Optimisation

KAUST, KSA

- Numerical linear algebra libraries
- Asynchronous tasking
- Deep Learning for Bio-Science

GW4

- ARM system tuning
- ARM ecosystem
 development
- Joint ARM, Cavium partnership



Coming up: LUMI and HLRS

CURRENT H2020 PROJECTS



WHAT IS A SUPERCOMPUTER?

Any of a class of extremely powerful computers. The term is commonly applied to the fastest highperformance systems available at any given time.

[A device for] processing of massively complex or data-laden problems using the concentrated compute resources of multiple computer systems working in parallel.

[a device to] handle and compute on volumes of data at speeds hundreds to millions of times faster than on a typical data center server

A supercomputer is a computer with a high level of performance as compared to a general-purpose computer.

A supercomputer is scientific instrument.

- folklore

A supercomputer is a device for turning compute-bound problems into I/O-bound problems.

- Ken Batcher

- Wikipedia

- HPE

- nimbix

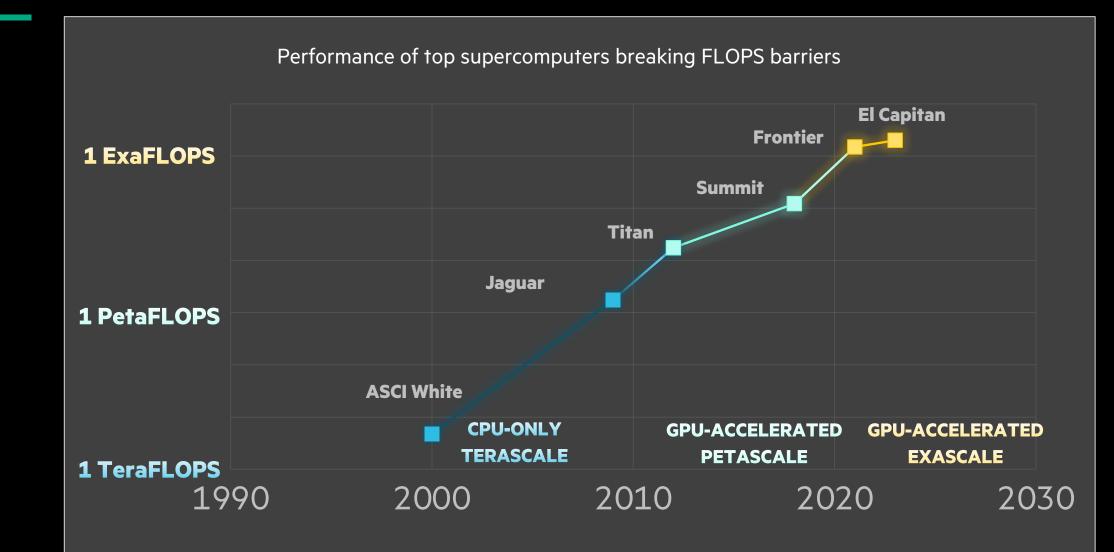
- Britannica

EXA..WHAT?

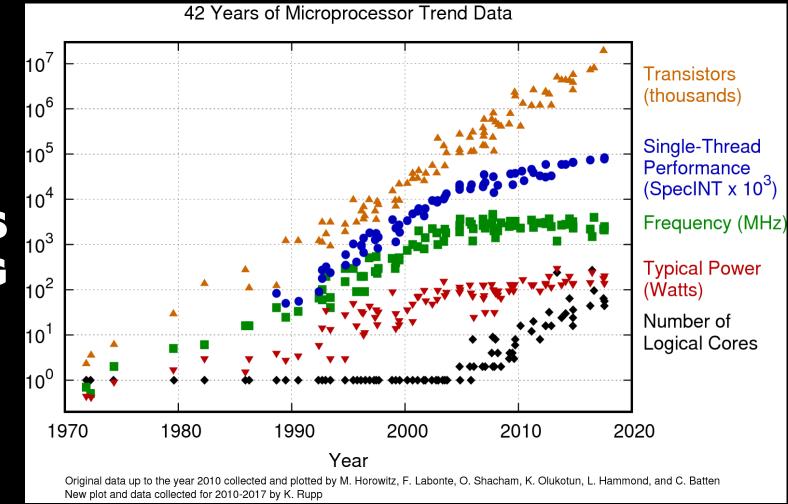
- Exascale computing: 10^{18} Floating Point Operations per second (FLOPS)
 - Measured by LINPACK:
 - solve Ax = b for dense A
 - using LU factorization with partial pivoting
 - with $\frac{2}{3}n^3 + O(n^2)$ operations
 - In double-precision IEEE floating point
- Theoretical peak performance R^{peak}
 - ignoring communication between compute units

Raspberry Pi-4B	13.5 GF
iPhone 11 A13	0.8 TF
Nvidia Titan V	110 TF

MAJOR LEAPS IN PERFORMANCE: 3 ERAS OF SUPERCOMPUTING



INGREDIENTS IN A CRISIS CURRENTLY HAPPENING



https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

MEMORY V.S. COMPUTATION: THEN AND NOW



Fugaku, 2020



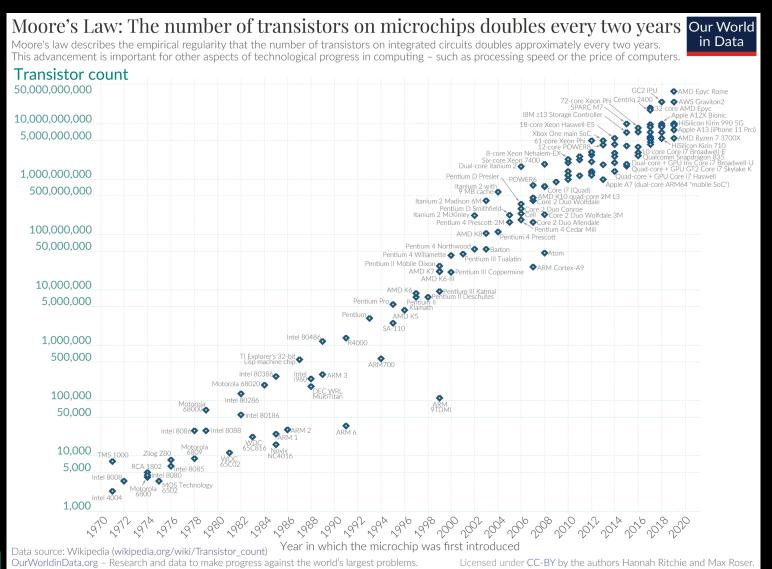
System Performance Perf/node Memory capacity /node Memory bandwidth /node Memory bandwidth / flop 160 MFLOPS 160 MFLOPS 8 MB 640 MB/s 4

537 PFLOPS 3.38 TFLOPS 32 GB 1024 GB/s 0.3 3356250000x 21125x 4000x 1600x 1/13 x



SEMICONDUCTOR WISDOMS (1)

Moore's Law



"The number of transistors in a dense integrated circuit (IC) doubles about every two years.

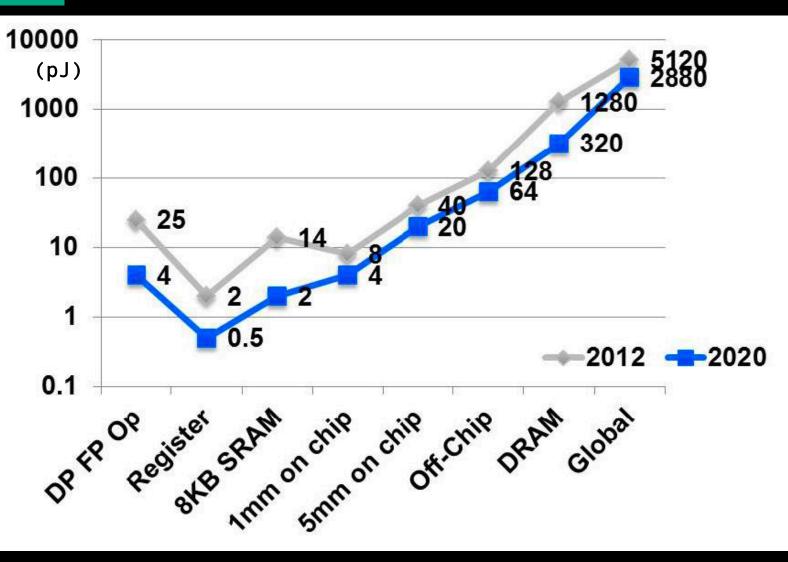
SEMICONDUCTOR WISDOMS (2) The end of Dennard Scaling (2006)

42 Years of Microprocessor Trend Data 10^{7} Transistors (thousands) 10⁶ Single-Thread 10⁵ Performance $(SpecINT \times 10^3)$ 10^{4} **Frequency** (MHz) 10³ Typical Power 10² (Watts) Number of 10 ogical Cores 10^{0} 1970 1980 1990 2000 2010 2020 Year Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten New plot and data collected for 2010-2017 by K. Rupp

"As transistors get smaller, their power density stays constant, so that the power use stays in proportion with area; both voltage and current scale (downward) with length"

https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/

DATA MOVEMENT COST



Energy cost, in picojoules (pJ) per 64-bit floating-point operation.

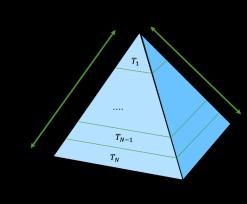
Note that the doubleprecision floating-point arithmetic (DP FP Op) energy cost is comparable to that for moving the same data 1mm– 5mm on chip.

That cost is dwarfed by the cost of any movement of this same data off chip.



MEMORY IS DIVERSE

- Caches L1,L2,L3
- DRAM
- GDRAM
- NUMA domains
- HBM/MCDRAM
- NVDIMM
- Node-local SSD
- • • •
- **Object Storage**
- GFS



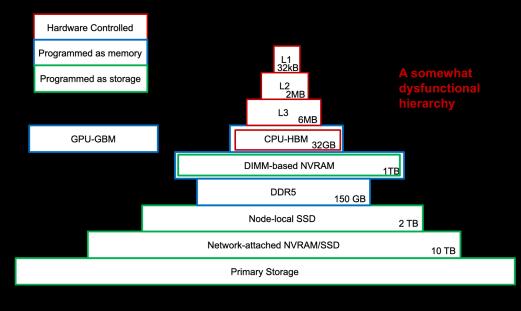
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ackage																		
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L3 (28MB)																		
Group0										Group0								
NUMANode L#0 P#0 (93GB)										NUMANode L#1 P#2 (94GB)								
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PU L#1 P#40	PU L#3 P#44	PU L#5 P#48	PU L#7 P#52	PU L#9 P#56	PU L#11 P#60				PU L#21 P#42	PU L#		PU L#25 P#50	PU L#27 P#54	PU L#29 P#58				
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PU L#13 P#64	PU L#15 P#68	PU L#17 P#72	PU L#19 P#76		eno4		eno2np	-111	PU L#31 P#62	PU L#		PU L#35 P#70	PU L#37 P#74	PU L#39 P#78				
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P#1 PU L#41	P#5 PU L#43	P#9 PU L#45	P#13 PU L#47	P#17 PU L#49	P#3 PU L#61	P#7 PU L#63	P#11 PU L#65			P#19 PU L#69				•	100	0162		
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L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB)	L1i (32KB) L	i (32KB)		• 2		MMI	mana	ged with		
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PU L#51	PU L#53	PU L#55	PU L#57	PU L#59	PU L#71	PU L#73	PU L#75	PU	L#77	PU L#79								
P#61	P#65	P#69	P#73	P#77	P#63	P#67	P#71		#75	P#79								
								-										

Host: leonide Date: Mon 16 Mar 11:23:55 2020

DATA MOVEMENT IS HARD AND A MAJOR PERFORMANCE BOTTLENECK

Is it still a hierarchy?

- Latency, bandwidth, capacity numbers not monotone anymore
- Some have separate address spaces
- Some not under our control



It's a dynamic (robust) vehicle routing problem with inventories and splittable resources. Contains

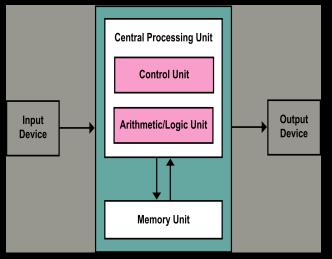
- Splittable flow
- Packing
- Job shop scheduling
- > Mathematically hard; hard to approximate
- Practically hard:
 - No uniform programming model
 - no system model to compute optimal schedules at scale



INGREDIENTS FOR A SOLUTION

Move computations, not data

Decouple instructions (code) and data movement Beware of von Neumann architecture bottleneck, in particular the word-by-word traffic paradigm



Count energy, not instructions

Remember when + and * were counted with different costs multipliers in CS101?

Our complexity classes don't capture instruction sets well where computation and data movement have exponentially different cost. **Recompute instead of reload**

Overlapping data movement and compute is no longer sufficient.

Ghosting, cache-oblivious or write-avoiding algorithms, architecture/topology-aware implementations are limited (and not future-proof)

Communication-avoiding algorithms are a niche topic.

Functional programming is the right abstraction: well-defined side-effect-free/closureconfined computations.

TASKING – A PARADIGM FOR DATA-AWARE PROGRAMMING

Data dependency driven programming abounds

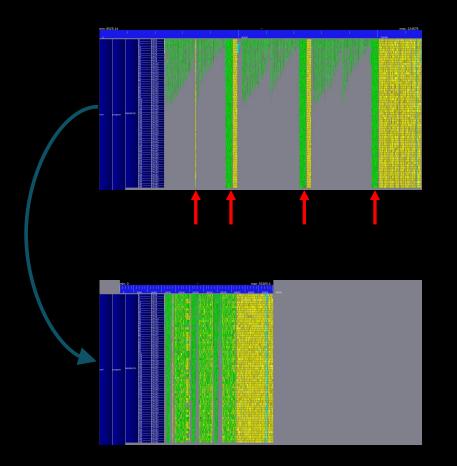
- At workflow level, explicit
 - Rise of heterogeneous coupled applications
 - Analytics, Systems Biology, Live "Big Data" processing
- In HPC
 - Parallel File System as backbone of implicit workflows
 - –Simulation-analysis coupling, checkpointing, archiving
 - -Coupler frameworks/middlewares

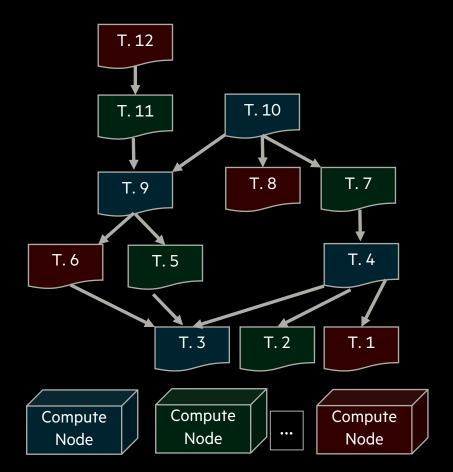
- In Programming Environment
 - Distributed tasking: HPX, PaRSEC, Legion, swift-lang, (StarPU), ...
 - On-node tasking: OMP tasking, StarPU; pthreads, ArgoBots, UPC
 - –Often lacking data locality information and data movement cost metrics
 - Functional paradigms entering mainstream languages (C++xx)
 - IO abstractions: Dataspaces, H5FDDSM, ADIOS2
- In Hardware abstraction
 - Dataflow architectures

DATA DRIVEN TASKING 101

- Decompose program into tasks that are coupled by input-output relations
 - A directed graph, tasks as nodes, data as arc labels, δ^+ , δ^- as outputs/inputs
 - Program execution:
 - Marking of initial tasks as 'ready to run'
 - Executing (some) 'ready-to-run' tasks
 - Marking successors of completed tasks as 'ready-to-run'
 - Acyclic in purely functional programming, cyclic with bounded number of cycle repeats for terminating nonpure programs
- Example: b = Ax decomposes into 2 + m tasks:
 - T_0 : Scatter rows of A
 - $T_1 \dots T_m$: m scalar product tasks $A_{i} \cdot x$
 - T_{m+1} : gather results into b

WHY?





SCHEDULING?

It's a kind of VRP, but then again not

Vehicle routing model Route code along data

- Data immutable
 - Explicit duplication operations allowed
- Hypergraph in bipartite representation
 - "substances" (data objects)
 - "reactions" (functional transformations)
 - A subset of transformations: data movement
- Transformation cost function (energy, time, ...)
 - Looks a lot like a Petri net

Job shop Scheduling: Assign tuples of data and code to compute resources

- Ordering constraints
- Machine-dependent execution times
- Data handling implicit in
 - Machine-dependent setup times
 - Sequence-dependent setup times
 - Reconfigurable machines: Data hierarchy access

Packing: Handling multiple concurrent workflows

- Inside one problem instance
 - 'Machines' have setup times, amortized cost
 - Competition for resources
- Across workflows
 - Non-cooperating users
 - Different/contradicting objectives (makespan, energy, ...)
- In time, on resources, partially splittable
- Often online

WHERE'S THE INSTANCE DATA?

System Monitoring

- Too coarse or too fine grained
- Based on hardware/software parameters that often are not suitable for a-priory models
- Often cannot be attributed to tasks
- Congestion vs. nominal data

Feedback profiling

- Not automatic
- Post-mortem
- Resulting models not sufficiently data-dependent

Machine models

- Nominal behavior/stochastic data
- Usable only at compiler or HPC workload manager level
- Very complex for modern large systems

Building a middleware (dataplane) that operates at application-defined object level permits

- data location awareness
- measuring at object level
- Compiler/application/workflow level optimal scheduling



https://www.maestro-data.eu/

OUTLOOK

- HPC is a great target for operations research techniques
 - Hardware and software system
 - Interconnects
 - Programming level
- Computational models disrupted
 - Data centricity
 - Heterogeneity up to the 'Cloud-to-Edge' level
- Many well-contained optimization problems and some extremely general ones
- After Exascale there'll be Zetascale, so there is no shortage of scalable problem instances

... and I've not even talked about **using** mathematical programming on HPC systems



THANK YOU

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